3.7 A 0.9V ΔΣ Modulator with 80dB SNDR and 83dB DR Using a Single-Phase Technique

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Low-power ΔΣ ADCs are required in a growing number of portable systems spanning from voice to biomedical applications. As CMOS technologies continue to evolve towards smaller geometries, new design techniques need to be developed to simplify the design of such ADCs, while improving energy efficiency and reducing die area. In this paper, these challenges are addressed by presenting a 2nd-order SC ΔΣM operating from a 0.9V supply that uses a single-phase clocking technique and a new amplifier-sharing scheme. The ΔΣM is fabricated in a 0.18μm CMOS process, occupies a die area of 0.06mm^2, dissipates 0.2mW from a 0.9V supply, and provides 80dB SNDR and 83dB DR over a 10kHz BW.

Figure 3.7.1 shows the scaled ΔΣM architecture. A 2nd-order non-cascaded topology is chosen due to its robustness against non-idealities. The coefficients *gx1*, *gx2*, *gdac1*, *gdac2* are, 1/4, 1/2, 1/3, and 1/3, respectively. The differential reference voltage, V_{REF}, is equal to 0.75V and is defined by V_{REFp}=0.875V and V_{REFn}=0.125V. The OSR is 256 and the nominal clock frequency, f_{CLK}, is 5.128MHz. The integrator (INT) outputs are designed for a differential voltage range of $1V_{pp}$, as shown in Fig. 3.7.1. The INTs are realized using a switched-opamp (SO) technique and two clock-bootstrapping (CBT) circuits are used at the input switches to enhance the linearity of the input sampling SC network, since the modulator input is operated at a common-mode (CM) voltage of $V_{DD}/2$. Two half-delay D-type FFs are used in the ΔΣM feedback path in order to compensate for the effect of the SO half-delay INTs on the ΔΣM transfer function. All coefficients are optimized to avoid the need of using any input CM dc-shifting capacitors, resulting in lower kT/C noise.

The block diagram of the fully differential ΔΣM circuit is shown in Fig. 3.7.2. Traditionally, 4 non-overlapping clock phases are used to drive the SC network in the INTs [1]. In this circuit, a single-phase clock, Φ_1, is used to drive all switches that are controlled by phases Φ_2, Φ_{2D} and $\Phi_{\overline{1D}}$. Likewise, switches driven by phases Φ_1, Φ_{1D}, and $\Phi_{\overline{2D}}$ are driven by a complementary phase $\Phi_{\overline{1}}$. Phases Φ_1 and $\Phi_{\overline{1}}$ are overlapping phases and, consequently, there is a certain fraction of time during which several switches conduct at the same time. This will produce a certain amount of charge that is lost when the charge is redistributed from the sampling and feedback capacitors into the integrating capacitors. However, as theoretically shown in [2], as long as the fall/rise-time delay, *td*, of the phases and the average equivalent conductance of the switches (g_{AVG}) during this overlapping time are both made small, the sampled signal degradation due to having various switches conducting simultaneously is negligible. With the evolution of CMOS technologies, the values of *td* and g_{AVG} are progressively being reduced. Hence, non-overlapping guard times might no longer be required in many SC circuits.

In practical CBT circuits, there is always an inherent delay between the input clock phase and the generated boosted output phase that drives the sampling switches. Hence, this single-phase scheme offers another design simplification by eliminating the need to have delayed versions of the sampling phases, necessary to avoid any signal-dependent charge injection. Furthermore, during the sampling operation of the SO circuits, the signal-dependent charge injection added by switching off the output stage of the opamp is very small, even if delayed phases are not used. The reason is that the signal swing at the input of the output stage of a two-stage opamp is always very small, and therefore, the amount of charge that must flow out of the channel region is practically signal-independent.

The two-stage opamp topology is presented in Fig. 3.7.3. It comprises two input PMOS trifferential-stages (blocks A11 and A12 comprising M_1, M_2, and M_c), folded into a common part (block AF comprising M_3 to M_5) and followed by two differential common-source output stages (blocks A21 and A22 comprising M_6 and M_7). CM input and output voltages, of $V_{CMI}=V_{LO}=V_{SS}$ and $V_{CMO}=V_{HI}/2=V_{DD}/2$ are used. Compensation is achieved by connecting capacitors C_{comp} to the sources of the NMOS cascode devices M_4 through switches S_1, when the corresponding output stage is switched ON. The output stages are turned ON/OFF by turning ON/OFF switches S_3 and OFF/ON switches S_2. The opamp is designed to be efficiently shared by both INTs, thus resulting in significant power and area savings. Since two input stages are available, A11 and A12, there is no need for using an input analog multiplexer as is done in [3], thus avoiding any memory parasitic effects that might degrade the performance of the INTs. Moreover, there is no extra burden in terms of circuitry and die area since when an input stage is being used by a given INT acting as a differential pair (the 3rd-input is switched-OFF through S_9), the other input stage (in trifferential mode) is also used to set the output CM to $V_{DD}/2$. This is done by adding the adjusting currents, I_{cmfb}, at the low-impedance nodes n_a. Two auxiliary SC networks comprising capacitors C_{CMS} and switches S_4 to S_8 are used to sense the CM at the outputs. For a target peak SNR of 84dB, the largest capacitance value is 2.4pF. In the chip implementation, 200fF unit capacitors are used.

The prototype IC is fabricated in a 0.18μm CMOS process using MIM capacitors. Only standard devices with $V_{Tn} \approx |V_{Tp}| \approx 0.5V$ are used and all transistors are biased in moderate inversion with V_{DSsat}=50 to 150mV. Figure 3.7.4 shows the chip layout. For comparison purposes, this IC includes, besides the described modulator, named ΔΣM-1, a second ΔΣM, named ΔΣM-2. ΔΣM-2 is a replica of ΔΣM-1 that uses a conventional 4-phases clocking scheme to drive the SC switches. ΔΣM-1 occupies a die area of only 0.06mm^2, while modulator ΔΣM-2 is 17% larger due to the phase generator block and the phase buses. Figure 3.7.5 shows the measured FFT for ΔΣM-1 and Fig. 3.7.6 displays the measured SNDR versus signal amplitude for both modulators. These measurements are made for a 2.5kHz signal frequency and 5MHz clock frequency. At 0.9V, ΔΣM-1 achieves 80dB SNDR, 82dB SNR, and 83dB DR over a 10kHz BW and dissipates 0.2mW from a 0.9V supply. Both modulators have similar SNR and DR but ΔΣM-1 shows a 3.5dB improvement in the SNDR due to the single-phase technique which improves the accuracy of the settling response. The key measurement results and a comparison between both ΔΣMs are summarized in Fig. 3.7.7.

References:

[1] D. G. Haigh, B. Singh, "A Switching Scheme for Switched-Capacitor Filters, Which Reduces Effect of Parasitic Capacitances Associated with Control Terminals," *Proc. ISCAS*, vol. 2, pp. 586-589, 1983.

[2] J. Goes et al., "Switched-Capacitor Circuits using a Single-Phase Scheme," *Proc. ISCAS,* pp. 3123 - 3126, May, 2005.

[3] V. Cheung, H. Luong, W. Ki, "A 1-V 10.7-MHz Switched-Opamp Bandpass ΔΣ Modulator Using Double-Sampling Finite-Gain-Compensation Techniques," *IEEE J. of Solid-State Circuits*, vol. 37, no. 10, pp. 1215-1225, Oct., 2002.

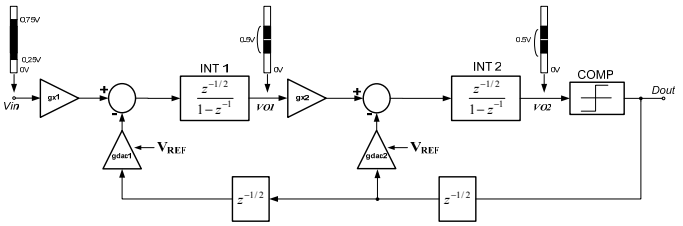

Figure 3.7.1: Scaled ΔΣM topology and expected single-ended voltage levels at the different nodes.

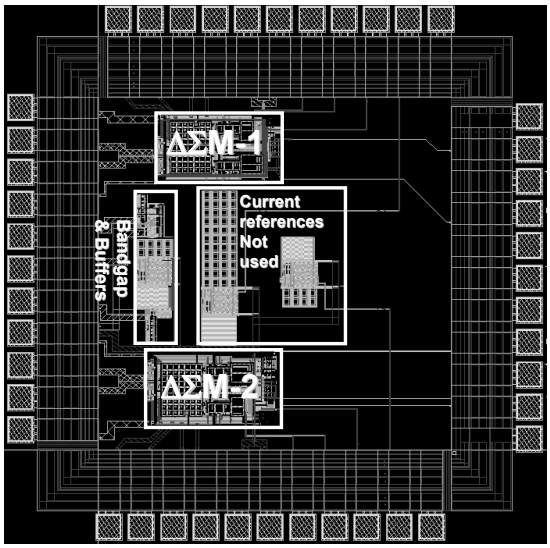

Figure 3.7.4: Chip layout.

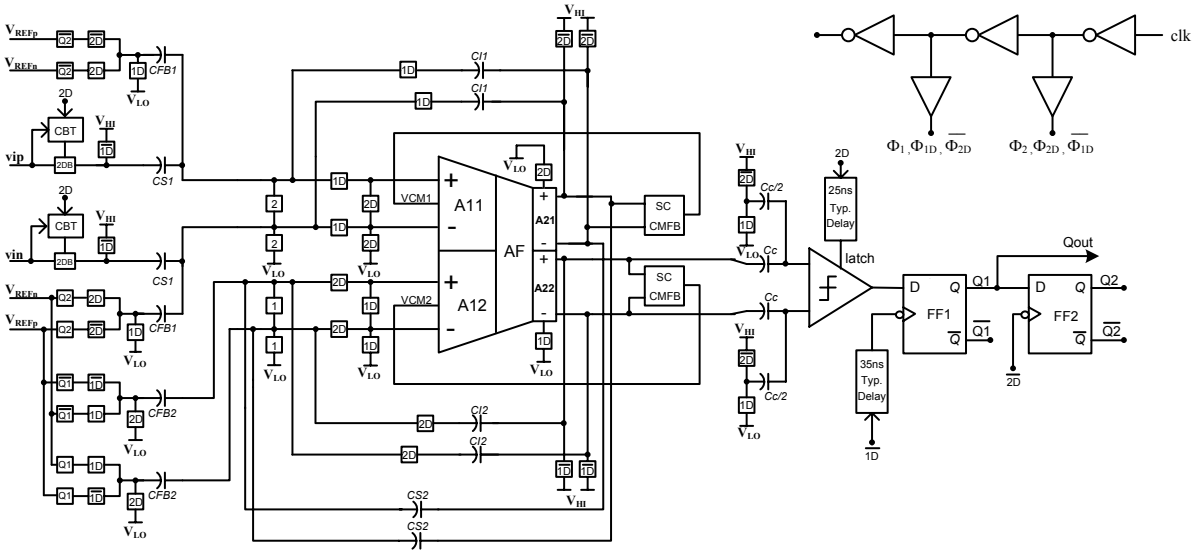

Figure 3.7.2: Second-order SO ΔΣM architecture with the proposed opamp-sharing scheme.

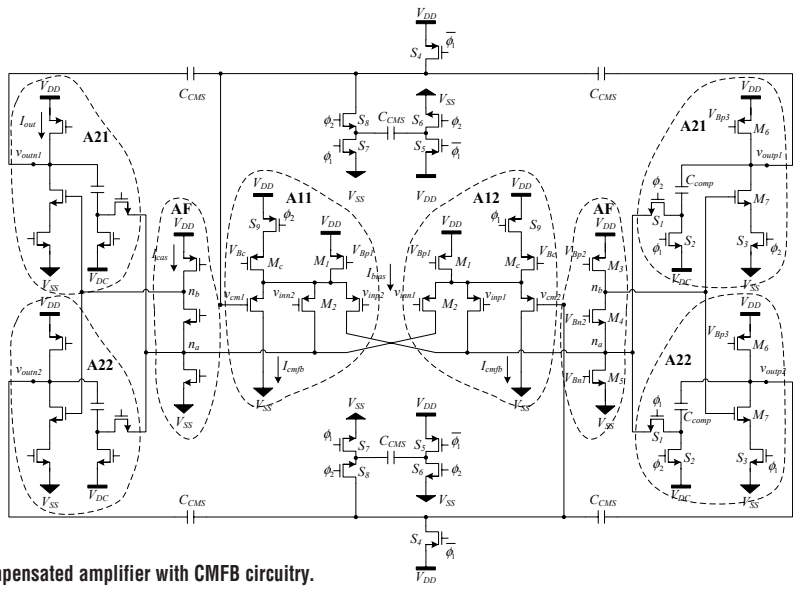

Figure 3.7.3: Two-stage cascode-compensated amplifier with CMFB circuitry.

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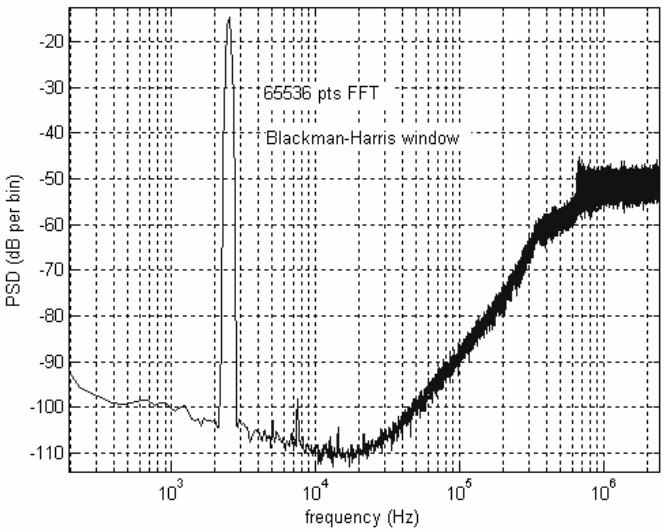

Figure 3.7.5: The 0.9V ΔΣM-1 output spectrum with an input signal of -5.5dBV.

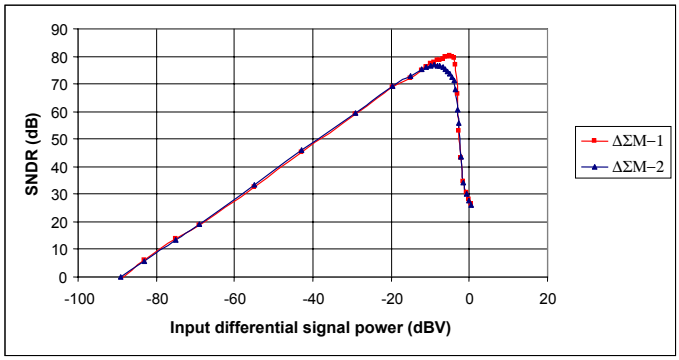

Figure 3.7.6: SNDR versus input signal level measured for ΔΣM-1 and for ΔΣM-2 and with VDD= 0.9V.

	ΔΣM-1	ΔΣM-2
Technology	0.18μm CMOS 1P-6M	
Supply Voltage	0.9V	
Clock frequency, F_{CLK}	5MHz	
OSR	256	
Signal BW	10kHz	
Power Dissipation	0.2mW	0.2mW
Die area	0.06mm^2	0.07mm^2
Peak SNR	82dB at -5.5dBV input level	
Peak SNDR	80.1dB at -5.5dBV input level	76.7dB at -9dBV input level
DR	83dB	

Figure 3.7.7: Key measured results.

